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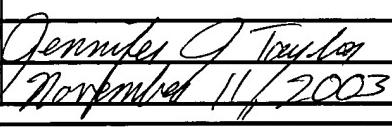
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Application Number Filing Date First Named Inventor Art Unit Examiner Name	10/624,716
	July 21, 2003
	Luan C. Tran
	2812
	Jennifer Kennedy
Total Number of Pages in This Submission	
	Attorney Docket Number
	MI22-2357

ENCLOSURES (Check all that apply)

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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual	Jennifer J. Taylor, Ph.D.; Reg. No. 48,711; Wells St. John P.S.	
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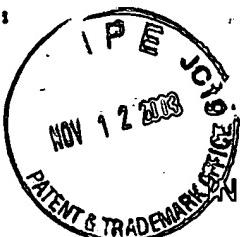
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EL979949902



THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 10/624,716
Filing Date July 21, 2003
Inventor Luan C. Tran
Assignee Micron Technology, Inc.
Group Art Unit 2812
priority Examiner Kennedy, Jennifer J.
Attorney's Docket No. MI22-2357
Title: Methods of Forming Semiconductor Constructions

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

References –See Attached Form PTO-1449

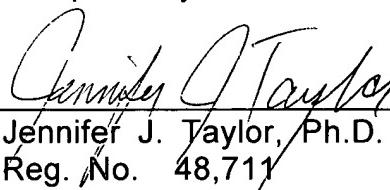
The attached form PTO-1449 is submitted in compliance with 37 CFR § 1.56. Copies of the cited art are included with the exception of U.S. patents and published U.S. applications (Official Gazette Notice: 05 August 2003). No admission is made regarding whether all the submitted references are prior art.

This Supplemental Information Disclosure Statement is being filed within three months of the filing date of the application or before the mailing date of a first Office Action, whichever occurs last. Therefore, no fee is believed to be required. However, in the event that a fee is required for filing this Supplemental Information Disclosure Statement, please charge the fee specified under 37 C.F.R. § 1.17(p) to Deposit Account No. 23-0925.

Respectfully submitted,

Dated: November 11, 2003

By:


Jennifer J. Taylor, Ph.D.
Reg. No. 48,711



U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE				ATTY. DOCKET NO. MI22-2357	SERIAL NO. 10/624,716
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Luan C. Tran	
				FILING DATE July 21, 2003	GROUP 2812

U.S. PATENT DOCUMENTS

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	6,144,079 A	11-2000	Shirahata et al.			
	AB	6,033,952	03-2000	Yasumura, et al.			
	AC	6,124,168	09-2000	Ong			
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							Yes	No
	AM	EP 0718881	06/96	EPO, Chan				
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	AO							
	AP							

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)

	AR		Watanabe, H. et al., <i>Novel 0.44μm² Ti-Salicide STI Cell Technology for High-Density NOR Flash Memories and High Performance Embedded Application</i> , IEEE 1998, pp. 36.2.1 - 36.2.4.				
	AS		Wolf, S., <i>"Silicon Processing for the VLSI Era"</i> , Vol. 2, pp. 632-635.				
	AT		MITSUBISHI ELECTRIC WEBSITE: Reprinted from website http://www.mitsubisielctric.com/r_and_d/tech_showcase/ls8.php on 3/29/2001: "8. Production Line Application of a Fine Hole Pattern-Formation Technology for Semiconductors", on 3/29/2001, 4 pgs				

EXAMINER	DATE CONSIDERED
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LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Luan C. Tran			
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Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
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							Yes
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	AR		CAHNERS SEMICONDUCTOR INTERNATIONAL WEBSITE: Reprinted from http://www.semiconductor.net/semiconductor/Issues/1999/sep99/docs/feature1.asp on 3/29/2001: "Resists Join the Sub- λ Revolution", 9 pgs.				
	AS		CAHNERS SEMICONDUCTOR INTERNATIONAL WEBSITE: Reprinted from http://www.semiconductor.net/semiconductor/Issues/1999/aug99/docs/lithography.asp on 3/29/2001: "Paths to Smaller Features", 1 pg.				
	AT		Wolf, S., "Silicon Processing for the VLSI Era, Vol. 1: Process Technology," Lattice Press 1986, pp. 434-437.				
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*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA	6,552,401 B1	04-2003	Dennison				
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	AC	US2002/0182829A1	12-2002	Chen				
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	AH							
	AI							
	AJ							
	AK							
	AL							
FOREIGN PATENT DOCUMENTS								
		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No
	AM							
	AN							
	AO							
	AP							
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)								
	AR		<i>"Session 18: Integrated Circuits and Manufacturing - DRAM and Embedded DRAM Technology," 2001 IEDM Technical Program, 2001 IEEE International Electron Devices Meeting, Dec. 4, 2001, reprinted 11/15/01 from http://www.his.com/~iedm/techprogram/sessions/s18.html, pp. 1-2.</i>					
	AS							
	AT							
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